Hall Ticket Number:

Code No. : 21613

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (ECE: CBCS) I-Semester Main Examinations, January-2019

(Embedded Systems & VLSI Design)

Digital IC Design

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Q.No.	Stem of the question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	What is sub-threshold slope? What is its effect on P_d and performance?	2	2	1	1,2
2.	List two important design metrics for evaluating a VLSI circuit performance and comment on their trade-offs.	2	2	1	1
3.	Implement OR/NOR function using Complementary Pass-transistor Logic.	2	2	3	2
4.	How do you compensate for the charge leakage in a dynamic logic NAND2 circuit?	2	3	3	2
5.	Distinguish a dynamic CMOS latch from a static CMOS latch, giving neat circuits.	2	2	3	1,2
6.	Give two sources of power-grid noise in a VLSI chip. How do you mitigate them?	2	3	4	3
7.	How does dual V_{th} transistor technique reduce power consumption in a VLSI system?	2	2	5	2
8.	Compare a carry bypass adder with a ripple carry adder in terms of speed and area.	2	2	5	2
9.	Draw a 1T DRAM cell. Draw its Read and Write timing diagrams.	2	2	6	2
10.	Draw a simple sense amplifier circuit used in RAM structures? Why is it necessary?	2	3	6	2
	Part-B (5 × 8 = 40 Marks)				
11. a)	Why are design abstraction levels important in VLSI design? Justify with an example.	4	3	1	3
b)	Estimate the propagation delay, t_{pd} and Noise Margins, NM_L and NM_H for skewed CMOS inverter sized as $(W/L)_P / (W/L)_N = (4/1)$.	4	3	1	2
12. a)	Compare Transmission Gate (TG) logic with pass transistor logic. Plot the R_{eq} vs V_{out} for a TG and interpret.	4	2	3	2
b)	Design an 8- input AND gate with an EE of 6 using pseudo-nMOS logic. If the parasitic delay of an n-input pseudo- nMOS NOR gate is (4n+2)/9, what is the path delay?	4	5	3	3
13. a)	Draw the schematic of a C^2MOS Master-slave register. Why is it not clock-overlap sensitive?	4	2	3	2
b)	A function log(|a+b|) is to be implemented using three modules, namely, adder, absolute value and log computers. Given t_{pd} of each of these modules is 10ns (approx) and the registers used have a set up time of 20 ps and t_{c-q} delay of 100 ps, compute the maximum clock frequency at which this system works correctly. By how much can you improve the performance by pipelining? What is the latency?	4	4	3	2

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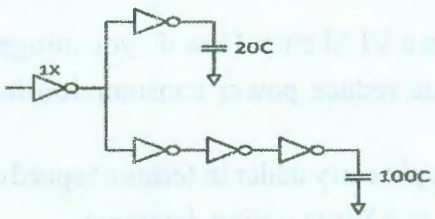
14. a)	Briefly explain the principle of operation of a Carry-Look ahead Adder (CLA) with the help of a conceptual diagram. How is the ripple effect eliminated? What are its limitations?	4	3	5	2
b)	A CMOS VLSI chip in 1.2V, 100 nm process has 200 million transistors, of which 180 million transistors are in memory arrays. (W/L) ratios of Logic and memory transistors are (6/1) and (2/1) with activities 0.1 and 0.05 respectively. Assuming the transistors have a gate capacitance of 2 fF/μm, estimate the dynamic power consumption per MHz of the system.	4	4	5	2
15. a)	Compare and contrast a 3T DRAM cell with a standard 6T SRAM cell with suitable schematics.	4	2	6	2
b)	Draw the architecture of a 128K SRAM organized as a 512 × 256 core array. Estimate the word-line capacitance assuming C_g = 2fF, C_{sd} = 0.5 fF and C_w = 0.2 fF.	4	5	6	3
16. a)	Define LE, BE and EE. Find the LE of a NAND4.	4	2	2	2
b)	A simplified clock distribution network is shown below. Assuming the bottom path with 100C is critical, size the inverters using LE technique. 	4	4	2	3
17.	Answer any ***two*** of the following:				
a)	SRAM DRV.	4	3	6	2
b)	4 bit Barrel Shifter.	4	2	5	1
c)	Standby Power Management in a VLSI Chip.	4	2	5	1

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	50%
2	Knowledge on application and analysis (Level-3 & 4)	37%
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	13%